What is Claimed is:

1. In a target processor, apparatus for storing a program counter address related to the generation of the a trigger signal, the apparatus comprising:

a trigger generation unit coupled to the plurality of event signal generation units, the trigger generation unit responsive to at least one preselected event signal for generating an associated trigger signal, the trigger generating unit also generating a trigger control signal;

a register, the register having program counter address related to the trigger signal applied thereto, the register storing the program counter address in response to a control signal generated by the trigger generation unit when the trigger signal is generated; and

a delay unit, the delay unit delaying application of the program counter address to the register.

2. The apparatus as recited in claim 1 further comprising a read bus, wherein a second control signal causes the contents of the register to be applied to the read bus.

3. The apparatus as recited in claim 1 wherein a state machine is an event generation unit.

4. The apparatus as recited in claim 1 further comprising:

a second register, the second register responsive to the control signal for storing indicia of the events signals.

5. The method of storing a program counter address related to the generation of a trigger signal, the method comprising:

generating a event signal for each predetermined event;

applying each event signal to a trigger generation unit;

when a predetermined event signal or combination of event signals is applied to the trigger generation unit, the trigger generation unit providing a trigger signal and a trigger control signal; and

applying the trigger control signal to the storage unit, the storage unit storing the program counter address resulting in the generation of the trigger signal in the storage unit in response to the trigger control signal.

6. The method as recited in claim 5 further comprising the step of delaying the program counter address applied to the storage unit.

7. The method as recited in claim 6 wherein the storage unit is a register.

8. The method as recited in claim 6 wherein a control signal applies the contents of the storage unit to a read bus.

9. The method as recited in claim 4 further comprising storing indicia of each event signal resulting in the trigger signal in a second register in response to the trigger control signals.

10. A target processor comprising:

a state machine, the state machine generating a first event signal in response to a configuration of the target processor;

at least one event detection unit, each event detection unit responsive to predetermined configuration of the target processing unit for generating a related event signal;

a trigger generation unit, the trigger generation unit generating trigger signal in response to at least one of the first and the related event signals, the trigger unit generating a trigger control signal when the a trigger signal is generated; and

a storage unit, the storage unit coupled to the program counter, the program counter applying address

signals to the storage unit, the storage unit storing a program counter address in response to the trigger control signal.

11. The target processor as recited in claim 10 further comprising a delay line, the delay line delaying the application of the program counter address to the storage unit for a predetermined period of time.

12. The target processor as recited in claim 10 further comprising a read bus coupled to the storage unit, the program counter address stored in the storage unit being applied to the read bus in response to a second control signal.

13. The target processing unit as recited in claim 11 wherein the storage unit is a register.

14. The target processor as recited in claim 11 further comprising a second register, the second storage unit having each event signal applied to at least one associated storage unit position, the storage unit storing applied signals in response to the trigger control signal.